AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of fabricating an active layer of a polycrystalline silicon thin film transistor, the method comprising ~~the steps of~~:

depositing a buffer layer on a substrate;

depositing an amorphous silicon layer on the buffer layer with a first ~~predetermined~~ thickness;

crystallizing the deposited amorphous silicon layer by using a laser to form a polycrystalline silicon layer;

etching the crystallized polycrystalline silicon layer to a second ~~predetermined~~ thickness thinner than the first thickness;

curing the etched polycrystalline silicon layer; and

patterning the cured polycrystalline silicon layer to form a semiconductor layer.

2. (Currently Amended) The method according to claim 1, wherein the first thickness is ~~the amorphous silicon layer is deposited with a thickness of~~ about 700 - 10000 Å.

3. (Original) The method according to claim 1, wherein the crystallizing uses an excimer laser.

4. (Original) The method according to claim 3, wherein an excimer laser crystalizing process uses one of an excimer laser process and a sequential lateral solidification process.

5. (Currently Amended) The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to the second [[a]] thickness according to a channel resistance, and wherein the second thickness is determined ~~the polycrystalline silicon layer has a thickness~~ to achieve a desired on-current drive for the thin film transistor.

6. (Previously Presented) The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched in order to achieve a process margin for etching a subsequent contact hole to contact a source/drain electrode and wherein the etched polycrystalline silicon layer is thicker than a defined thickness.

7. (Original) The method according to claim 1, wherein the polycrystalline silicon layer is etched to a thickness of about 100 - 600 Å.

8. (Currently Amended) The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to the second [[predetermined]] thickness by using a chemical mechanical polishing process.

9. (Currently Amended) The method according to claim 1, wherein the crystallized polycrystalline silicon layer is etched to the second [[predetermined]] thickness by using an etch-back process.

10. (Original) The method according to claim 1, wherein the etched polycrystalline silicon layer is cured at a temperature of about 400 – 500 °C.

11. (Original) The method according to claim 1, wherein the etched polycrystalline silicon layer is cured using a laser annealing process.

12. (Original) The method according to claim 1, wherein the etched polycrystalline silicon layer is cured using a rapid thermal annealing process.

13. (Currently Amended) The method according to claim 1, further comprising ~~the steps of~~:

forming a first insulating film on the formed layers;

depositing a metal film on the first insulating film and forming a gate electrode by patterning the metal film;

forming a second insulating film on the layers on which the gate electrode is formed;

forming a first contact hole and a second contact hole to the semiconductor layer by etching the first and second insulating films on the semiconductor layer so that a portion of the semiconductor layer is exposed;

depositing a metal film on the second insulating film and patterning the metal film to form a source electrode and a drain electrode connected electrically to the semiconductor layer through the first contact hole and the second contact hole;

forming a passivation film on the formed source/drain electrode;

forming a third contact hole in the passivation film to the drain electrode; and

forming a pixel electrode connected electrically to the drain electrode through the third contact hole by depositing a transparent conductive film on the layers and patterning the transparent conductive film.

14. (Currently Amended) A method of fabricating an active layer of a polycrystalline silicon thin film transistor, the method comprising ~~the steps of~~:

depositing an amorphous silicon layer on a substrate at a first [[predetermined]] thickness;

crystallizing the deposited amorphous silicon layer to form a polycrystalline silicon layer using a sequential lateral solidification (SLS) method;

reducing the thickness of the crystallized polycrystalline silicon layer to a second [[predetermined]] thickness thinner than the first thickness, wherein the second thickness is at least determined by an on/off current ratio of the polycrystalline thin film transistor; and

patterning the reduced polycrystalline silicon layer to form a semiconductor layer.

15. (Currently Amended) The method according to claim 14, wherein the first thickness is ~~the amorphous silicon layer is deposited at a thickness of~~ about 700 - 10000 Å.

16. (Original) The method according to claim 14, wherein crystallizing uses an excimer laser.

17. (Currently Amended) The method according to claim 14, further comprising curing the polycrystalline silicon layer having the second thickness ~~16, an excimer laser crystalizing process uses one of an excimer laser process and a sequential lateral solidification process~~.

18. (Currently Amended) The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to <u>the second</u> [[a]] thickness according to a channel resistance, and wherein <u>the second thickness is determined</u> ~~the polycrystalline silicon layer has a thickness~~ to achieve a desired on-current drive for the thin film transistor.

19. (Previously Presented) The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced in order to achieve of a process margin for etching a subsequent contact hole to contact a source/drain electrode, and wherein the polycrystalline silicon layer is thicker than a defined thickness.

20. (Original) The method according to claim 14, the polycrystalline silicon layer is reduced to a thickness of about 100 - 600 Å.

21. (Currently Amended) The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to <u>the second</u> ~~a predetermined~~ thickness by using a chemical mechanical polishing process.

22. (Currently Amended) The method according to claim 14, wherein the crystallized polycrystalline silicon layer is reduced to <u>the second</u> ~~a predetermined~~ thickness by using an etch-back process.

23. (Currently Amended) The method according to claim 14, further comprising ~~the steps of~~:

forming a first insulating film on the formed layers;

depositing a metal film on the first insulating film and forming a gate electrode by patterning the metal film;

forming a second insulating film on the layers on which the gate electrode is formed;

forming a first contact hole and a second contact hole to the semiconductor layer by etching the first and second insulating films on the semiconductor layer so that a portion of the semiconductor layer is exposed;

depositing a metal film on the second insulating film and patterning the metal film to form a source electrode and a drain electrode connected electrically to the semiconductor layer through the first contact hole and the second contact hole;

forming a passivation film on the formed source/drain electrode;

forming a third contact hole in the passivation film provided on the drain electrode; and

forming a pixel electrode connected electrically to the drain electrode through the third contact hole by depositing a transparent conductive film on the layers and patterning the transparent conductive film.